



FACULTY OF ENGINEERING AND THE ENVIRONMENT
DEPARTMENT OF MINING ENGINEERING
DEPARTMENT OF GEOMATICS AND SURVEYING ENGINEERING
DEPARTMENT OF METALLURGICAL ENGINEERING

ELECTRICAL PRINCIPLES
EMG1203 / EMN1203 / ESG1206
Final Examination Paper

June 2025

This paper consists of 6 pages

Time Allowed: 3 hours

Total Marks: 100

Examiner: Mr. K. Garapo

INSTRUCTIONS

1. This paper contains TWO sections.
2. Answer ALL FOUR questions in SECTION A and any THREE of the five questions in SECTION B.
3. Each question in SECTION A carries 10 marks and each question in SECTION B carries 20 marks.
4. Show all your workings.
5. Illustrate your answers, where appropriate, with clearly labeled diagrams.
6. Start each question on a new page.

Additional requirements:

Scientific calculator

SECTION A (Answer all four questions)

Question 1

Refer to the graph shown in **Figure 1** to answer the following questions:

- a) Determine the peak voltage V_p of the alternating-current component of the signal S_0 . [2 marks]
- b) Determine the period T of the signal S_0 . [2 marks]
- c) Determine the frequency f of the signal S_0 . [2 marks]
- d) Determine the root mean square voltage V_{rms} of the alternating-current component of the signal S_0 . [2 marks]
- e) Determine the direct voltage offset V_{dc} in signal S_0 . [2 marks]

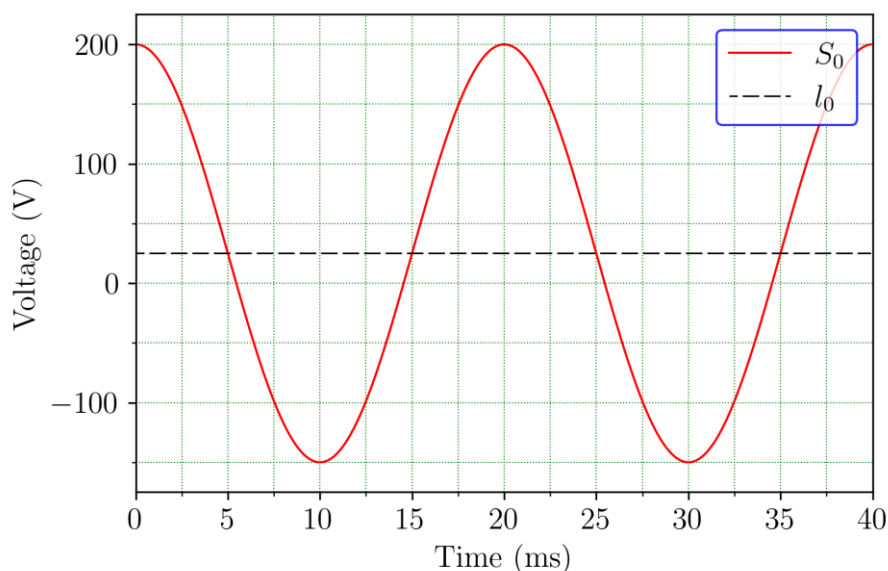


Figure 1. Graph of an alternating voltage signal S_0 . The signal S_0 is symmetrical about the line l_0 .

Question 2

- a) Draw the circuit of the OPAMP differentiator. [5 marks]
- b) Derive the expression for the output voltage phasor \bar{V}_{out} of the OPAMP differentiator in terms of the complex input impedance \bar{Z}_{in} , the complex feedback impedance \bar{Z}_f and the input voltage phasor $\bar{V}_{in} = V_m \angle 15^\circ$. [5 marks]

Question 3

- a) State the two nominal steady-state main grid electricity-transmission voltages in Zimbabwe. [2 marks]
- b) State the following:
- maximum allowable steady-state per-unit (pu) main grid voltages during normal operation in Zimbabwe. [1 mark]
 - minimum allowable steady-state per-unit (pu) main grid voltages during normal operation in Zimbabwe. [1 mark]
- c) Use the per-unit values you gave in b) to calculate the following:
- maximum voltage values for each of the steady-state main-grid voltages you gave in a). [2 marks]
 - minimum voltage values for each of the steady-state main-grid voltages you gave in a). [2 marks]
- d) State the maximum transmission voltage in Zimbabwe. [2 marks]

Question 4

The delta and star circuits shown in **Figure 2** are equivalent. Determine the values of R_1 , R_2 and R_3 , given that $R_a = 220 \Omega$, $R_b = 470 \Omega$ and $R_c = 300 \Omega$. [10 marks]

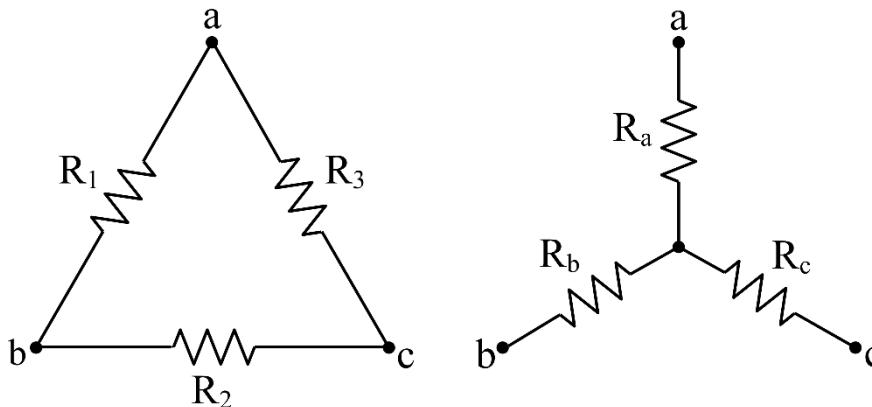


Figure 2. Equivalent delta and star resistor networks.

SECTION B (Answer any three of the five questions only)

Question 5

Refer to the circuit shown in **Figure 3** to answer the following questions:

- a) Determine the input voltage phasor \bar{V} . [2 marks]
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- b) Determine the current phasor \bar{I} . [8 marks]
- c) Determine the complex power \bar{S} delivered in the circuit. [4 marks]
- d) Determine the apparent power S delivered in the circuit. [3 marks]
- e) Determine the power factor PF for the circuit. [3 marks]

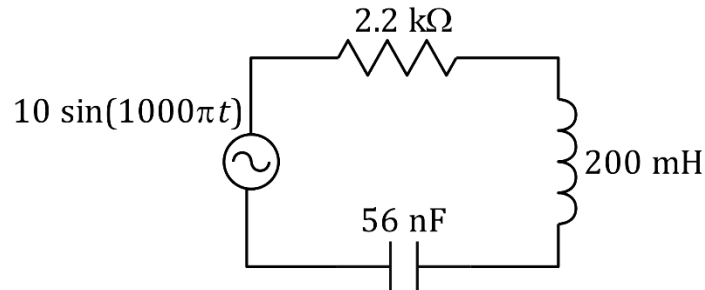


Figure 3. Series RLC circuit.

Question 6

- a) Apply Norton's theorem to determine the Norton equivalent of the circuit shown in **Figure 4**, given that Z_{LOAD} is the load of interest in the circuit. [15 marks]
- b) Determine the value of the load impedance \bar{Z}_{LOAD} required to draw maximum power from the voltage source. [5 marks]

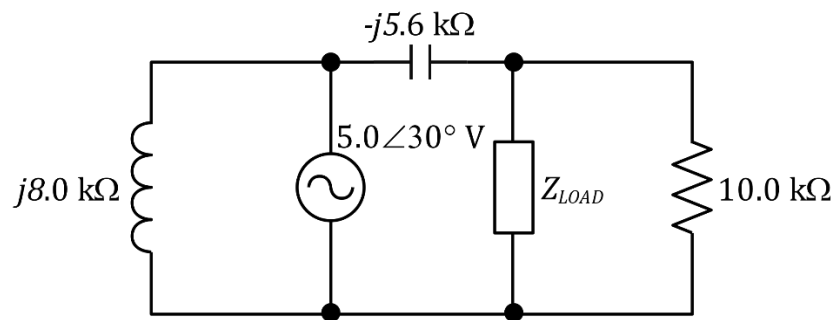


Figure 4. Planar alternating current circuit.

Question 7

Figure 5 shows three transistor-logic (TL) and transistor-transistor-logic (TTL) gates, labelled (a), (b) and (c). For each gate, the input voltages are labelled **A** or **B**; the output voltages are labelled **X**. Voltages from 0 V to 0.8 V are assigned the logic level 0 and voltages from 2 V to 5 V are assigned the logic level 1. For each of the three logic gates do the following:

- i. Construct a truth table in terms of logic levels 0 and 1.

- ii. State the standard name and draw the standard circuit symbol.
- iii. State whether the gate is a basic or a universal logic gate. [20 marks]

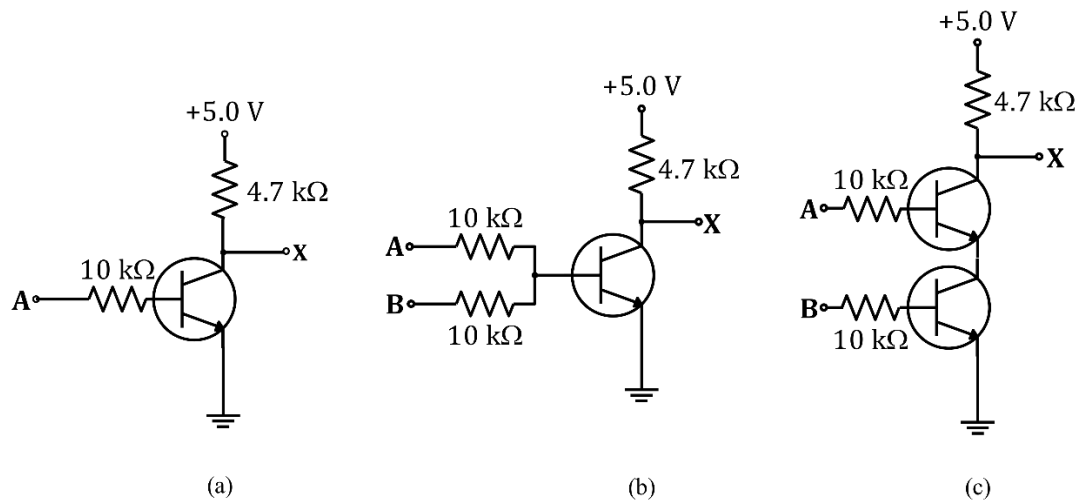


Figure 5. Three transistor logic gates.

Question 8

- a) Refer to *Figure 6* to answer the following questions:
- Determine the time constant τ . [2 marks]
 - Determine the time, after switching on the circuit, it will take the capacitor to charge to 8.0 V from an initial value of 0 V? [4 marks]
 - Determine the time, after switching on the circuit, it will take the current in the circuit to fall to half of its initial value? [4 marks]

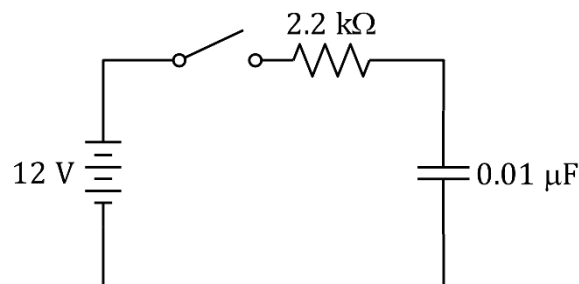


Figure 6. Series RC circuit.

- b) Refer to *Figure 7* to answer the following questions:
- Determine the time constant τ . [2 marks]
 - Determine the time, after switching on the circuit, it will take the voltage across the inductor to fall to 4.0 V? [4 marks]

- iii. Determine the time, after switching on the circuit, it will take the current in the circuit to rise to half of its final value? [4 marks]

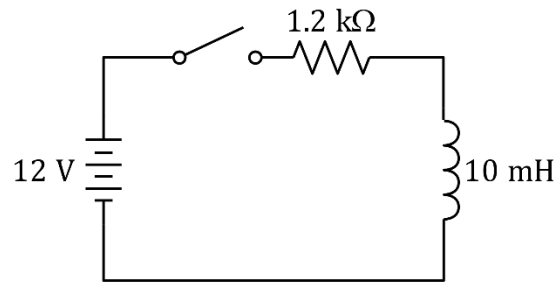


Figure 7. Series RL circuit

Question 9

Refer to the circuit shown in **Figure 8** to answer the following questions:

- Apply node-voltage analysis to determine the voltage at each of the two essential nodes. [6 marks]
- Determine the current flowing through the $10\ \Omega$ resistor from the voltages obtained in a). [2 marks]
- Apply the superposition theorem to determine the current flowing through the $10\ \Omega$ resistor. [6 marks]
- Apply the mesh-current analysis to determine the current flowing through the $47\ \Omega$ and $22\ \Omega$ resistors. [6 marks]

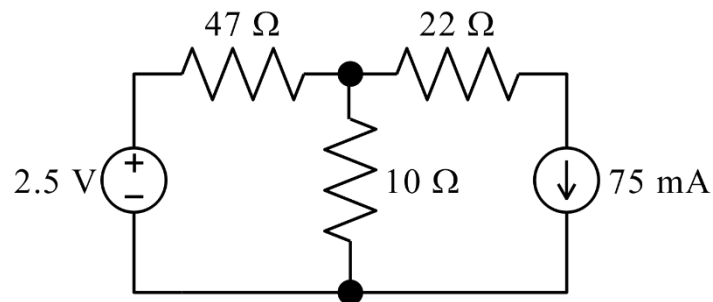


Figure 8. Planar circuit consisting of two meshes and two essential nodes.